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GLOBALLY CONVERGENT HOMOTOPY METHODS FOR THE DC OPERATING POINT PROBLEM*

ROBERT C. MELVILLE†, LJILJANA TRAJKOVIĆ‡, SAN-CHIN FANG†, AND LAYNE T. WATSON+

Abstract. Accurate and efficient computer simulation of a proposed design for an integrated circuit ("chip") is essential because of the difficulty and expense of building prototypes for such devices. The transistors and diodes in such circuits are modeled with nonlinear equations, hence simulation of integrated circuits requires the solution of systems of nonlinear equations involving hundreds or even thousands of variables. This paper discusses the application of probability-one homotopy methods to various systems of nonlinear equations which arise in circuit simulation. The so-called "coercivity conditions" which are required for such methods are proved using concepts from circuit theory. The theoretical claims of global convergence for such methods are substantiated by experiments with a collection of examples which have proved difficult for commercial simulation packages which do not use homotopy methods. Moreover, by careful design of the homotopy equations, the performance of the homotopy methods can be made quite reasonable.

Key words. direct current bias, electronic circuit simulation, electronic circuit steady-state, globally convergent homotopy, nonlinear equations, probability-one homotopy

AMS(MOS) subject classifications. 94C05, 68U20, 65H10

1. Introduction–an overview of electronic circuit simulation. Programs for the simulation of electronic circuits have been available since the mid 1960's [39], [20] (see [27] for a survey of early work in simulation), however the development of integrated electronics ("chips") has provided a tremendous impetus for work in circuit simulation. It is difficult or impossible to build a prototype of a circuit that will be fabricated on a silicon wafer. The only real test of a proposed design is to actually make a batch of chips at a cost somewhere between one thousand to one hundred thousand dollars, depending on the complexity of the design. The slightest mistake in the design of the chip, even one connection out of place, can invalidate the entire chip and force a costly redesign. Hence, computer simulation techniques become important for exercising a design before committing it to silicon.

In this section we provide a very brief overview of circuit equations, and of a typical analog circuit simulator, emphasizing parts that solve systems of nonlinear algebraic equations. The rest of our paper describes the application of globally convergent homotopy methods to these systems. As the name implies, numerical implementations of globally convergent homotopy methods exhibit an exceptionally wide domain of convergence. However, these methods are *not* applicable to arbitrary systems of nonlinear equations. Certain "coercivity" conditions are needed to argue that solutions to the homotopy equations cannot become unbounded. In §2, we demonstrate

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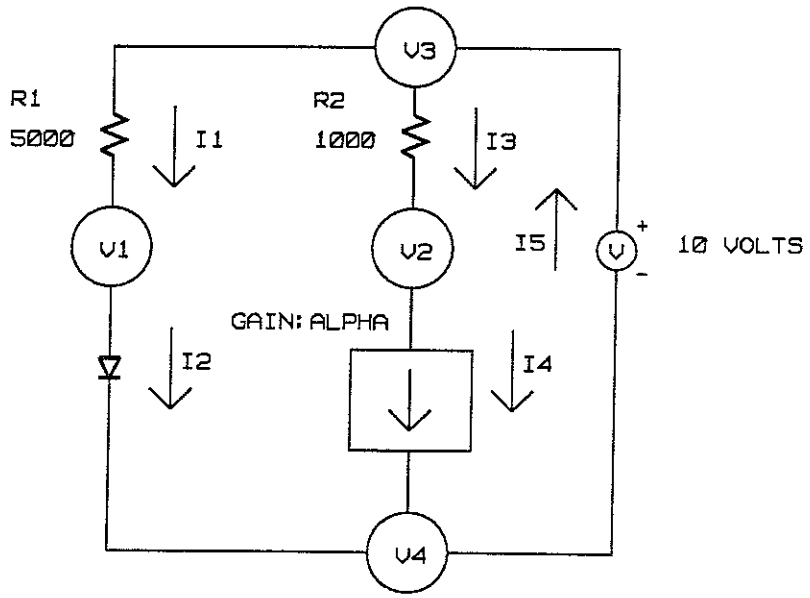

FIGURE 1. *An electric circuit.*

that the required coercivity conditions are, in fact, quite natural for equations that arise in circuit simulation. In §3, we describe various homotopies for solving systems of nonlinear equations. In §4, we extend these methods to a two-point boundary value problem that formulates so-called *steady state* equations for electronic circuits. In §5, we describe the practical implementation of a variety of homotopies for finding the direct current bias and the steady-state solutions of electronic circuits. Finally, in §6 we cite some related work.

1.1. Circuit equations. An electronic circuit (network) may be viewed as a directed graph. A vertex of the graph is called a *node*, and an edge of the graph is called a *branch*, or occasionally, a *link*. A voltage V_k is associated with each node of the graph and a current I_j with each branch. The current I_j associated with branch j is positive if it flows in the direction of the branch and negative if it flows in the reverse direction of the branch. The *voltage drop* across a branch between nodes $k1$ and $k2$ is the difference $V_{k1} - V_{k2}$, where V_{k1} is the voltage associated with node $k1$ and V_{k2} is the voltage associated with node $k2$.

A set of equations that describes the circuit is generated from three relationships:

- *constitutive relations* that are algebraic relationships among the currents and voltages imposed by particular devices in the circuit;
- *Kirchhoff's Current Law* that states that the sum of the currents, I_j, over the branches incident to a node is zero (I_j is positive if it flows into the node j and negative if it flows out of the node j);
- *Kirchhoff's Voltage Law* that states that the sum of voltage drops around any closed loop of the circuit is zero.

Figure 1 shows a five-node circuit containing a voltage source, two resistors, a diode, and a current amplifier. The nodes are indicated by circles, with the associated

voltage variable inside the circle. Each branch is labeled with a current variable and an arrow showing the direction of the current flow in the branch. Resistor R1 imposes the constraint $I_1 = (V_3 - V_2)/5000$; likewise R2 imposes the constraint $I_3 = (V_3 - V_2)/1000$. The diode imposes the constraint $I_3 = I_D(V_1 - V_4)$, where $I_D(V_1 - V_4)$ is a nonlinear function to be described later. The current amplifier imposes the constraint $I_4 = \alpha I_2$, where α is a constant called the *gain* of the amplifier. The current amplifier is an example of a *coupling element*, because it imposes a constraint that involves other branches in the circuit. Circuits without coupling elements are relatively simple. As we will see later, diodes and coupling elements allow us to model transistors.

These relationships, together with the Kirchhoff laws, generate the following system of equations:

$$\begin{aligned}
I_1 &= (V_3 - V_1)/5000, \\
I_2 &= I_D(V_1 - V_4), \\
I_3 &= (V_3 - V_2)/1000, \\
I_4 &= \alpha I_2, \\
I_1 + I_3 - I_5 &= 0, \\
I_1 - I_2 &= 0, \\
I_3 - I_4 &= 0, \\
I_2 + I_4 - I_5 &= 0, \\
V_3 - V_4 &= 10.
\end{aligned}$$

The above system of simultaneous equations is larger than necessary; for example, knowing V_1 and V_4 allows one to immediately infer a value for I_2, hence for I_4. A variety of methods are available for selecting an independent system of equations for a circuit [44]. The alternatives are compared on the basis of programming ease and, especially for large circuits, numerical stability. In this paper, we have chosen a particularly simple formulation for the circuit equations called the *(pure) nodal equations*. They are written in the following manner: Choose one node of the circuit as the reference or *ground* node which is fixed at 0 V by definition. Each branch consisting of a voltage source (such as the branch from V_3 to V_4 in Figure 1) must be connected to the ground node. Now, introduce voltage variables for all nodes *except* the ground node and the ungrounded end of each voltage source. Let there be n such nodes in the circuit. Write a system of n equations in n unknowns that expresses the Kirchhoff current law at each node of the circuit for which a voltage variable has been introduced.

Figure 2 shows the circuit of Figure 1, redrawn; note the change in notation for the unknown voltages. The two unknowns, x_1 and x_2, are the voltage drops across the diode and the current amplifier, respectively. Because current variables have been eliminated, it is convenient to assume the currents flowing "away" from a node along all branches incident to the node, no matter what the sign of the branch currents actually are. For example, the current flowing away from Node1 to Node3 is $(x_1 - 10)/5000$ and the current flowing away from Node1 to Ground is $I_D(x_1)$. The nodal formulation

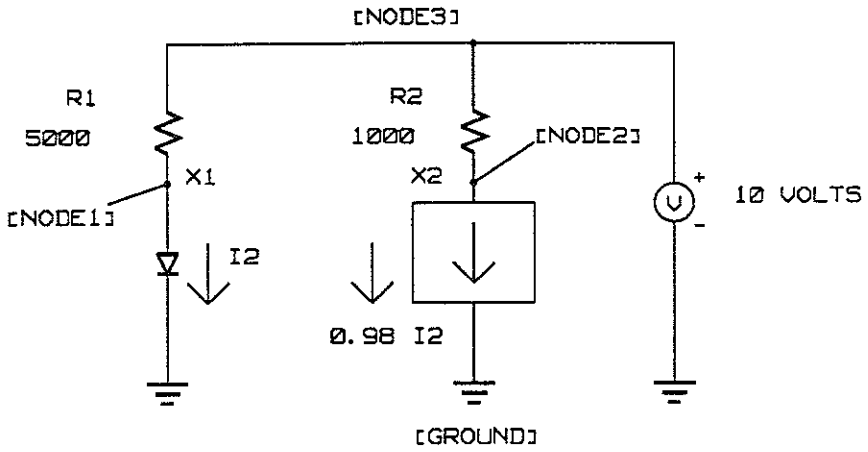

FIGURE 2. *Circuit for nodal equations.*

generates the following system of two equations in two unknowns for the circuit of Figure 2:

$$(x_1 - 10)/5000 + I_D(x_1) = 0,$$
$$(x_2 - 10)/1000 + \alpha I_D(x_1) = 0.$$

Such a system can be written as $F(x) = 0$, where x is an n-dimensional column vector of real numbers. An important special case is a circuit consisting of linear resistors, independent voltage sources, and current amplifiers, which is called a *linear circuit* because F takes the form $F(x) = Ax + b$, where A is an n by n matrix and b is an n-dimensional column vector. The term *affine circuit* might be more accurate.

Available matrix techniques allow the solution of linear circuits of dimension ten thousand or more. However, the introduction of nonlinear components, such as diodes, makes the solution of circuit equations much more difficult. Practical simulators employ a more sophisticated formulation of equations, such as the *modified nodal* formulation [29], that introduces current variables. The nodal formulation is adequate for the purposes of this paper.

The above discussion has been limited to circuits in which each node voltage is constant over time. A solution to such a circuit is variously called a *DC solution*, an *operating point*, or a *bias point.*

1.2. Inside a circuit simulator. Solution of circuit equations is automated by programs called *circuit simulators.* A typical circuit simulator has three major components—the input interface, the numerical engine, and the model library.

Consider how a simulation program would treat the simple nonlinear circuit of Figure 2. The circuit is described in a file provided as an input to the simulator:

```
*Comment -- Example Circuit
V Node3 Ground 10 Volts
R1 Node3 Node1 5000 Ohms
R2 Node3 Node2 1000 Ohms
D Node1 Ground DefaultModel
H Node2 Ground (Node1 Ground) 0.98
```

```
.dc op
.end
```

Node names follow the notation of Figure 2. Component types are distinguished by a convention based on the first letter of the name. The last field of each component line gives a "value" for the component parameter, such as 5000 Ω for resistor `R1`. The current amplifier is connected between nodes `Node2` and `Ground`, and is coupled to the current flowing from `Node1` to `Ground` with a gain of 0.98. The command line `.dc op` instructs the simulator to calculate the DC operating point of the circuit. The input interface reads this file and generates a data structure that describes the interconnection of components. Typically, a "subcircuit" mechanism is provided so that larger circuits can be built in a hierarchical fashion. For a nonlinear component, such as the diode, the user specifies a *model name*. This causes the simulator to reference a particular subroutine that computes the nonlinear response of the device.

After this data structure has been generated, the numerical engine is called to build and solve a system of equations, depending on the type of analysis the user has requested. For each node in the circuit, an equation is constructed by considering all components connected to that node. These equations take the rather simple form of a sum of terms, where each term is a call to a model subroutine (for a nonlinear device), a constant generated by a voltage source, or a linear combination of currents and voltages generated by resistors and current amplifiers. The final system of equations might have a few hundred variables for a medium sized circuit, and up to ten thousand variables for a large circuit. In either case, the Jacobian matrix of the system is sparse, and generally not symmetric.

The numerical engine references the model library for characteristics of the nonlinear devices in the circuit. For the diode, there is an exponential relationship between voltage x across the device (considered the stimulus) and current I_D through the device (considered the response) [22]:

$$I_D(x) = I_s \left(e^{x/V_T} - 1 \right). \tag{1}$$

Here, I_s and V_T are constants that depend on a particular choice of the diode type. The device model also computes the derivative dI_D/dx and should include some "current-limiting" mechanism. A practical value for V_T is 0.025 V. Therefore, rather small values of x, such as 2 V, can generate currents on the order of millions of amperes. Such currents do not have physical meaning, so a test is included in the model subroutine to keep the output currents within reasonable bounds. A careful implementation should preserve continuity of the derivatives at the boundary of the limiting regions. C^2 continuity is even better; more than C^2 is rarely needed. A model subroutine based on an equation such as (1) is called an "analytic model". An alternative technique is to take measurements from an actual device, and fit the sample points with a spline interpolating functions. Both approaches are used in commercial simulators.

In practice, robust solution of the operating point equations for even small circuits (ten or fewer components) can be difficult. A plot of (1) shows an extremely sharp knee as the diode starts to conduct around 0.7 V. This sharp nonlinearity explains some of the difficulties encountered in the numerical computation of the bias point. However, things get much more interesting with the inclusion of *transistors*. A transistor, the

key nonlinear component in integrated circuits, can be modeled using a combination of diodes and current amplifiers. A qualitative difference between circuits with and without coupling elements is shown by the following facts: a circuit consisting of voltage sources, linear (positive) resistors, and diodes possesses a unique DC operating point [19]. However, if transistors are allowed, the circuit can have multiple solutions. A circuit consisting of voltage sources, resistors, diodes, and transistors is an example of a *nonlinear resistive circuit.* Analysis of such circuits is still a topic of current research (see, for example, [26], [64]).

In the above example, there is no notion of time. Circuit simulators can also formulate systems of first-order ordinary differential equations that calculate the response of the circuit to time-varying stimuli as an initial value problem. At the initial time point for such a simulation, each time-varying stimulus can be viewed as having a fixed value. The DC operating points or bias points of this circuit at the initial time point provides the starting point for the integration of the differential equations. Therefore, DC operating points computation is necessary even for a time-domain simulation.

In special applications, a designer is interested in the *steady state* response of a circuit with a periodic stimulus. This is the time domain response after any initial transients have died out. In §4, we will formulate the steady state problem as a two-point boundary value problem. We will apply globally convergent homotopy methods to a systems of algebraic equations which result from discretizing the differential equations on a mesh of time points over one period of the stimulus.

2. Coercivity conditions for circuit equations. A number of elegant mathematical results concern solutions to systems of equations that satisfy certain "boundedness" conditions. Perhaps the best example is the Brouwer fixed point theorem [9] which states that a continuous map f from a convex compact set into itself must have a fixed point; i.e., for some x^* in the set, $f(x^*) = x^*$. Why might one think that the Brouwer fixed point theorem would be applicable to the DC operating point problem? The intuition that such is the case is based on the following fact about nonlinear resistive circuits (at least, those that arise in practical integrated circuit designs). At the DC operating point of such a circuit, each node voltage is bounded in absolute value by the sum of the absolute values of the voltage sources in the circuit [65]. A circuit with this property is called *no-gain.* In other words, if the circuit has n nodes, and we imagine the sum of the absolute values of the voltage sources normalized to the range $[0, 1]$, then the operating point is an element of the unit n-cube. This fact is no surprise to designers of electronic circuits, although a rigorous proof of this assertion is not trivial.

The no-gain property is intrinsic to real transistors, but may or may not be preserved in a circuit simulator, depending on transistor models. As an example, consider the circuit of Figure 3, which shows a typical bias configuration for a single transistor amplifier stage.

A transistor has three terminals called the *collector*, *base* and *emitter*, and, as stated above, can be modeled using a combination of diodes and current amplifiers. Figure 4(a) shows the circuit of Figure 3 redrawn with an overly simple model of a transistor. The diode is described by equation (1). The current flowing through the controlled source is a constant α_F times the current through the diode. Values for

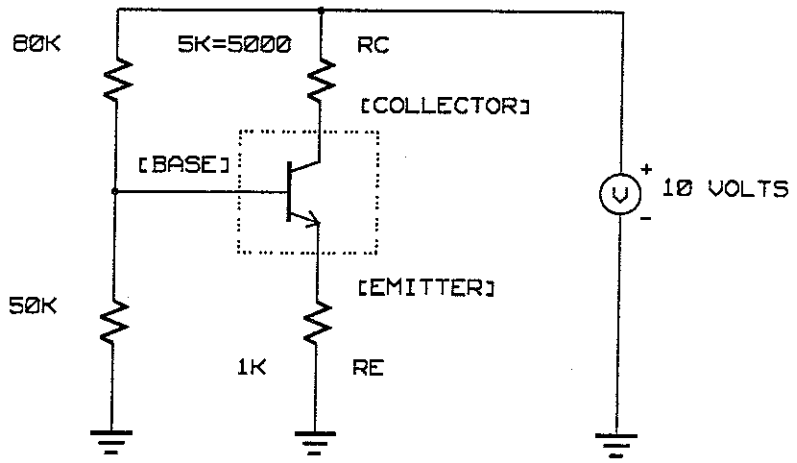

FIGURE 3. *One transistor bias circuit.*

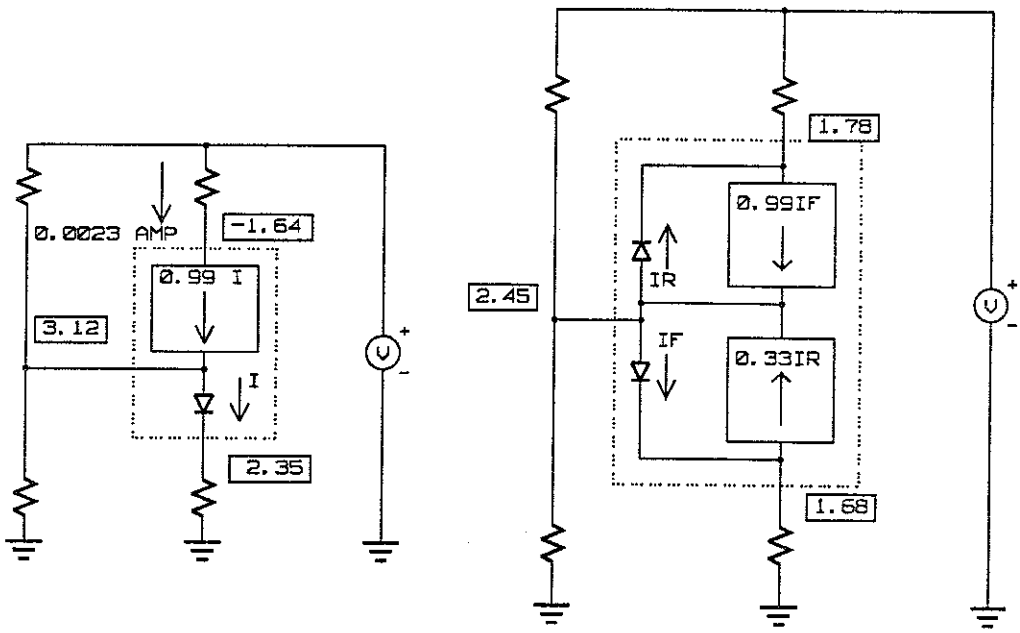

FIGURE 4. *Two models of a transistor.*

α_F range from 0.90 to 0.999 for practical transistors. The node voltages for the DC operating point are enclosed in rectangles at each node, and certain branch currents are indicated by arrows. Because more than 2.0×10^{-3} A flows through resistor RC, Ohm's law states that the solution voltage at the collector node must be *negative.* In fact, by adjusting the values of RC and RE, almost any negative voltage could be achieved at this node! A practicing circuit designer will immediately dismiss these solutions as invalid, even though the model using a single diode and current amplifier is sometimes used. The problem is that the simple transistor model does not capture the *saturation behavior* of a real transistor.

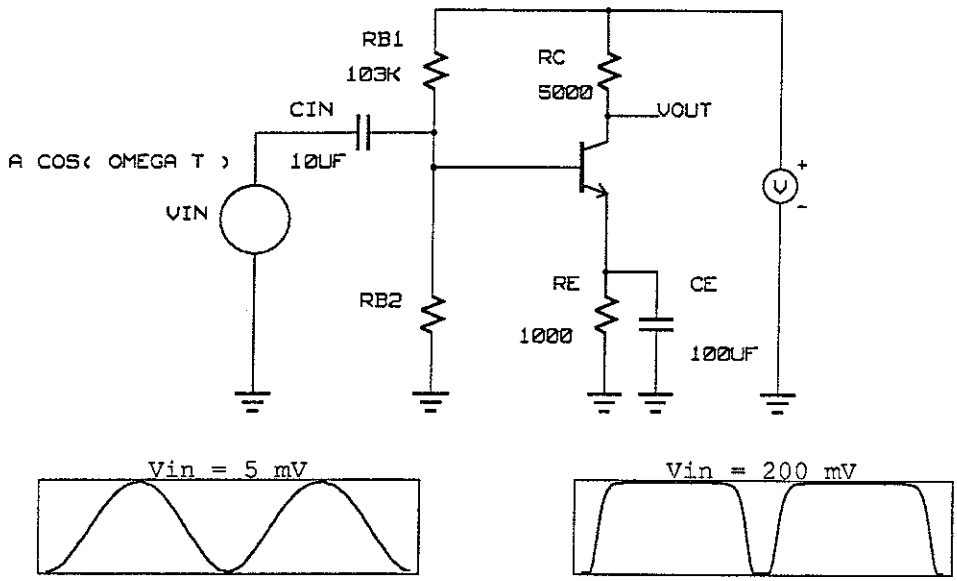

FIGURE 5. *Amplifier circuit.*

A more accurate model is shown in Figure 4(b). This model, due to Ebers and Moll [22], includes a second diode and a current source which come into play as the collector voltage gets close to the base voltage. The action of the second source is to cancel some of the current from the first source and keep the terminal voltages from becoming negative. The solution voltages for the circuit with the Ebers-Moll model agree with experimentally observed voltages (and, indeed, are in the range [0,10] V).

This kind of boundedness property extends to the time-domain behavior of electronic circuits. Figure 5 shows a simple amplifier circuit with sinusoidal stimulus generated by the voltage source labeled `VIN`. The voltage across this source is a function of time of the form $A\cos(\omega t)$, where A, with dimension *Volts*, sets the amplitude of the stimulus and ω, with dimension *radians/second*, sets the frequency. The "output" of the circuit is the waveform on the collector node voltage of the transistor. Two output waveforms are shown for two different amplitudes of `VIN`. The first waveform is almost sinusoidal, differing from the input only in amplitude. However, as the amplitude of the input signal increases, at some point the transistor saturates and the output waveform *clips*, so that its peak-to-peak amplitude remains bounded by the supply voltage.

Despite the historical appeal of the Brouwer fixed point theorem, and the body of knowledge about the no-gain property, we have found the following theorem [32] more general and easier to apply to circuit equations.

THEOREM 1. *Let F be a continuous mapping from $\mathbf{R}^n$ into $\mathbf{R}^n$. Suppose that $x^T F(x) \geq 0$ for all $x \in \mathbf{R}^n$ such that $\|x\| = r$, where r is a fixed positive real number. Then F has a zero x^* such that $\|x^*\| \leq r$.*

A proof of this theorem for the one-dimensional case is obvious, since it simply states that F is zero at an end point of the interval $[-r, +r]$ or has a sign change on the interval. A proof in higher dimensions may be obtained by reduction to the Brouwer fixed point theorem [32].

The nodal formulation of circuit equations specifies a sum of currents for each node. The result is a system

$$\begin{aligned} F_1(x_1, \ldots, x_n) &= 0, \\ F_2(x_1, \ldots, x_n) &= 0, \\ &\vdots \\ F_n(x_1, \ldots, x_n) &= 0, \end{aligned}$$

where the dimension of x_i is voltage and the dimension of F_i is current. Thus, the dimension of the inner product $x^T F(x)$ is *power*.

An circuit element is *passive* if it does not generate power [67]. This can be stated in mathematical terms by considering the voltage v_k across each element and the current i_k flowing into the element. If the sum $\sum i_k v_k$ over all elements is always nonnegative, then the device is *passive*. Passivity is a less restrictive condition than the no-gain property introduced earlier.

Among the electronic devices introduced so far, linear (positive) resistors, diodes, and transistors are passive. The current amplifier is not passive, however, the particular arrangement of diodes and current amplifiers in the Ebers-Moll transistor model is passive [23]. Any interconnection of passive components is passive. This lets us evaluate the inner product condition for the nodal equations of a nonlinear resistive circuit. The particular values of circuit parameters establish a radius of a ball in $\mathbf{R}^n$ such that for any vector of node voltages x on this ball, the inner product $x^T F(x)$ is a sum of powers which is nonnegative. If we appeal to passivity rather than the no-gain property, then, in general, the radius of this ball will be larger than the sum of the absolute values of the independent voltage sources, and might be difficult to calculate. However, applications of Theorem 1 do not require the *knowledge* of the radius, only its existence. A detailed exposition of this argument appears in [51].

Therefore, a passivity argument can be made for an electronic circuit consisting of independent voltage sources, resistors, diodes, and transistors. This covers almost all practical cases. Occasionally, designers use voltage amplifiers to model operational amplifiers. A voltage amplifier delivers an output voltage μv_{in}, where μ is a constant and v_{in} is a voltage drop across some branch in the circuit. The graph of the input/output relationship of such a device would be a straight line of slope μ extending to infinity in either direction. Suppose μ is large, say 1000. Then an input voltage of 1 V generates an output voltage of 1000 V. Again, common sense about electronic circuits says that an operational amplifier built using transistors and operated from +12 V and -12 V supplies cannot generate an output voltage of 1000 V. Any practical operational amplifier exhibits *limiting* behavior at its output. That is, the output is indeed equal to μv_{in} over some range of v_{in}, but beyond that range, the output voltage is bounded by the positive and negative power supply values. When a voltage amplifier is modified to model this limiting behavior (which is a more accurate model of an operational amplifier) the inner product condition of Theorem 1 can be satisfied at a certain radius r which may depend on the limits set for the voltage amplifiers.

So far, our discussion of passivity has been limited to the case of nonlinear resistive circuits, i.e., circuits with no notion of time. In a later section of this paper, we discuss passivity for the time-domain response of a circuit.

3. Homotopies for the DC operating point problem. The general homotopy paradigm involves embedding the equations to be solved, $F(x) = 0$, in a system of equations of one higher dimension, $H(x, \lambda) = 0$, with the introduction of one more variable λ, called the *homotopy parameter* or *continuation parameter*. Typically, λ is restricted to the range $[0, 1]$ and the embedding is done so that the augmented system $H(x, 0) = 0$ is easy to solve and reduces to the original system when $\lambda = 1$, i.e., $H(x, 1) = F(x)$.

Starting from the solution to $H(x, 0) = 0$, one follows a connected set of points (x, λ) such that $H(x, \lambda) = 0$ until $\lambda = 1$. In traditional continuation methods [34], sometimes called *monotonic continuation*, a functional relationship is assumed between x and λ, so that there is a unique value $x(\lambda)$ such that $H(x(\lambda), \lambda) = 0$ for each $\lambda \in [0, 1]$. An important extension of the continuation paradigm is to *arc-length continuation* [31], in which both x and λ are thought of as functions of arc length s along a connected set of points such that $H(x(s), \lambda(s)) = 0$. Now, s is advanced to a value s^* such that $\lambda(s^*) = 1$.

Continuation methods, either monotonic or arc-length, are well known in circuit simulation, either for finding an operating point [10], [14], [15], [11], [43], [53], [54], [68], [69], [70], [35], [63], [74] or for calculating a DC transfer curve [18]. For example, one approach to the operating point problem is to multiply each voltage source in the circuit by λ. When $\lambda = 0$, the circuit has an obvious solution in which each node voltage is 0 V. A continuation process is used to advance λ to 1, where a point x^* such that $H(x^*, 1) = 0$ represents a solution to the circuit with all voltage sources at their desired values.

Continuation of the supply voltage is a good example of *natural parameter* continuation, as discussed in [56], because the continuation parameter has an obvious physical interpretation. In this section we describe some theoretical work of Chow, Mallet-Paret, and Yorke [13], who have given a class of methods which can be proven to have very desirable numerical properties. The methods presented in [13] are called *artificial parameter homotopy* methods to distinguish them from traditional continuation methods, either monotonic or arc-length. Artificial parameter methods, also known as *globally convergent probability-one methods*, require a full rank condition on the derivative of the embedding H, which is not always satisfied by natural parameter embeddings. Our work concentrates on the artificial parameter approach.

Consider the scheme for continuation in the values of the voltage sources, using continuation in the arc-length parameter s. Mathematically, this process is described by a system of equations

$$\begin{aligned} H_1(x_1(s), \ldots, x_n(s), \lambda(s)) &= 0, \\ H_2(x_1(s), \ldots, x_n(s), \lambda(s)) &= 0, \\ &\vdots \\ H_n(x_1(s), \ldots, x_n(s), \lambda(s)) &= 0, \end{aligned}$$

where x_1 through x_n represent the node voltages. The parameter $\lambda \in [0, 1]$ multiplies the value of each independent voltage source. The *zero set* of H is

$$H^{-1}(0) = \{(x(s), \lambda(s)) \mid \lambda \in [0, 1] \text{ and } H(x(s), \lambda(s)) = 0\},$$

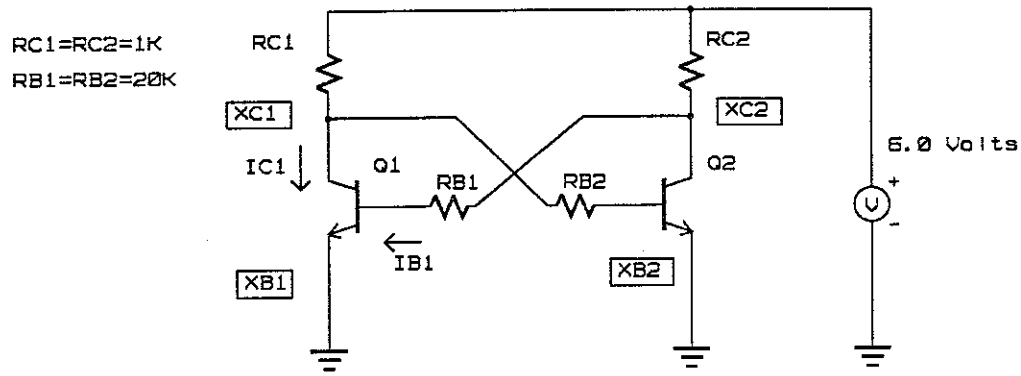

FIGURE 6. *Flip flop.*

which is typically a union of curves in $\mathbf{R}^{n+1}$. Given a starting point in the zero set (certainly available at $\lambda = 0$) one can think of moving along a component of the zero set as tracing the trajectory of an initial value problem. Numerical procedures for carrying out this kind of *curve tracking* will be described later.

Unfortunately, this continuation scheme is not always robust. For certain circuits, at a critical point on the zero set, the solution trajectory will attempt to split (bifurcate). If the curve following procedure is unlucky enough to hit the bifurcation point, or a sufficiently small neighborhood of it, the Jacobian matrix of H will become rank deficient. Bifurcations are not easy to deal with numerically. Note that a circuit may have a unique operating point at the *final* value of all the supplies, yet still have multiple operating points at their intermediate values. In such a case, the success or failure of source stepping will be sensitive to the relative rate at which the various sources are turned on. Such behavior is reported in [72].

Consider the flip-flop of Figure 6. This is a circuit with three DC operating points. However, if the value of the voltage source is set to zero, then the circuit has a unique solution, with all voltages equal to zero. Let $x = (xc_1, xb_1, xc_2, xb_2)^T$ be the vector of node voltages. The following equations represent the voltage source continuation embedding for this circuit:

$$
\begin{aligned}
H_1(x,\lambda) &= (xc_1 - \lambda\mathtt{VCC})/\mathtt{RC1} + (xc_1 - xb_2)/\mathtt{RB1} + ic_1, \\
H_2(x,\lambda) &= (xb_1 - xc_2)/\mathtt{RB2} + ib_1, \\
H_3(x,\lambda) &= (xc_2 - \lambda\mathtt{VCC})/\mathtt{RC2} + (xc_2 - xb_1)/\mathtt{RB2} + ic_2, \\
H_4(x,\lambda) &= (xb_2 - xc_1)/\mathtt{RB1} + ib_2,
\end{aligned}
$$

where H is a mapping from $\mathbf{R}^{n+1}$ into $\mathbf{R}^n$, with $n = 4$. The Jacobian matrix for H has dimension $n \times (n+1)$ and can be evaluated for any particular $(x,\lambda) \in \mathbf{R}^{n+1}$. Does this matrix have full rank (i.e., rank 4) for *all* points in the zero set of H? The answer is no; the symmetry in the circuit generates a bifurcation at a critical point in the zero set with $\lambda \approx 0.1135$. Then $\lambda\mathtt{VCC} \approx 0.68$ V, just enough to "turn on" the base-emitter junctions of the two transistors. The rank of the Jacobian matrix of H was monitored by performing a singular value decomposition of the Jacobian matrix [49]. At the critical value for λ mentioned above, the smallest singular value drops to approximately 2×10^{-14}, indicating a rank deficiency.

A rather different approach to the formulation of embeddings is taken in [13], resulting in artificial parameter homotopies. Under certain conditions, the zero set of such homotopies can be shown to contain a smooth curve that leads to a solution with bounded arc length. Bifurcations and other numerical difficulties do not occur. In particular, Chow, et al. [13] consider solving a system of equations $F(x) = 0$, where $F : \mathbf{R}^n \rightarrow \mathbf{R}^n$ satisfies the inner product condition of Theorem 1. They impose the additional condition that F be C^2, and consider the following homotopy for finding a zero of F:

$$\rho_a(x, \lambda) = \lambda F(x) + (1 - \lambda)(x - a), \tag{2}$$

where $a = (a_1, ..., a_n)$ is a fixed element of $\mathbf{R}^n$. Note that a solution to $\rho_a(x, 0) = 0$ is trivial, and a solution to $\rho_a(x, 1) = 0$ is a zero of F. Following the homotopy paradigm the easy problem, "solve $(x - a) = 0$", is deformed in a continuous manner into the desired problem, "solve $F(x) = 0$". The zero set for (2) is the set $\Gamma_a = \{(x, \lambda) | \lambda \in [0, 1)$ and $\rho_a(x, \lambda) = 0\}$.

The theory developed in [13] shows that with the additional assumption that F is C^2, then for *almost all* choices of a with $\|a\| \leq r$, Γ_a contains a smooth path emanating from $(a, 0)$ and terminating at a point $(x^*, 1)$, where $F(x^*) = 0$. The term "almost all" means that the set of starting points that do not generate successful trajectories has measure zero in $\mathbf{R}^n$. This property of the artificial parameter methods is a consequence of a version of Sard's theorem [46]. Thus, the a vector provides an element of random choice in the procedure for finding a zero of F. Each different choice for a provides a different possible path to a zero of F; "most" such paths are successful. The algorithm, then, for finding a zero of F, is to pick such an a at random (which fixes a value for $x_0 = x(0)$), then solve an initial value ODE problem to generate the solution trajectory emanating from $(x_0, 0) = (a, 0)$.

Watson, et al. [56], [57], [58] have done careful numerical implementation of an algorithm that can follow the solution trajectory of (2). Code is available in a package called `HOMPACK`. The implementation in `HOMPACK` requires the user to supply a subroutine to evaluate F and its Jacobian matrix. Given a starting point a, `HOMPACK` tracks the solution trajectory of (2) for $\lambda \in [0, 1]$. Because the set of bad starting points has measure zero, a random choice of a has zero probability of hitting one. In this sense, the algorithm for finding a zero of F is globally convergent. Of course, a computer implementation has only a finite approximation to the real numbers so that every set of floating point numbers has measure zero. Nontheless, our experiments with probability-one homotopy algorithms, as implemented in `HOMPACK`, indicate exceptionally robust convergence, provided that the device models are smooth enough.

3.1. A formulation of the operating point problem. The *nodal formulation* presents the operating point problem as a system of nonlinear equations $F(\mathbf{x}) = 0$, where $\mathbf{x}$ is a vector of node voltages. Let there be n nodes, and let x_k denote the voltage at node k. $F_k(x_1, \ldots, x_n)$ will be an equation for the sum of currents flowing into node k through all the branches connected to that node. The system F has been shown to satisfy the inner product condition if all the devices (other than the voltage sources) are passive. Thus, the homotopy (2) can be used to find an operating point for the circuit.

In fact, $\rho_a(x,\lambda) = 0$ has an interesting physical interpretation. For an arbitrary node k, imagine connecting a resistor in series with a voltage source to the ground. Let the value of the voltage source be a_k, and the value of the resistor be $\lambda/(1-\lambda)$. The nodal equation for node k is

$$\sum_{j=1}^{m} I_j = \frac{(1-\lambda)}{\lambda}(a_k - x_k), \tag{3}$$

where there are m branches connected to node k in the original circuit, carrying currents $I_1, \ldots, I_m$. Recognizing that the current summation on the left-hand side of (3) is $F_k(x)$ as previously defined, we see that (3) is equivalent to (2).

Note that the value of the resistor is 0 for $\lambda = 0$. Hence, the node voltage is forced to the value a_k at $\lambda = 0$. Then, as λ approaches 1, the value of the resistor approaches infinity, and the initial source is decoupled from the circuit.

The physical interpretation of the homotopy also provides intuition about why the homotopy should be bifurcation free for almost all choices of an a vector. Consider the flip-flop of Figure 6. The operating point equations for this circuit have three solutions, corresponding to transistor `Q1` on and transistor `Q2` off, `Q2` on and `Q1` off, and both transistors on. As discussed above, the zero curve of the supply continuation equations for this circuit must have a bifurcation. On the other hand, imagine connecting a resistor and voltage source combination to the two collector nodes. Let the voltage sources have values a_1 and a_2. Now, sweep the value of the resistors from zero to infinity. The only choice of (a_1, a_2) that will hit the bifurcation is $a_1 = a_2$; any other pair of starting values will steer the circuit to one mode or the other. Given a random choice of (a_1, a_2), the probability of hitting $a_1 = a_2$ is zero. In practice, such pathological cases can easily be circumvented.

Consider again the natural parameter homotopy proposed for the flip-flop in §3. `HOMPACK` *was* able to follow the zero curve of this homotopy to a solution at $\lambda = 1$, even though there is a bifurcation in the zero curve—the curve tracking procedure was lucky enough to "hop over" the bifurcation point on the zero curve. However, what operating point was found by following the zero curve of the natural parameter homotopy? Answer: the *unstable* operating point at which both transistors conduct equal amounts of current. This operating point is of little or no interest to a designer. On the other hand, the introduction of the random vector moves the zero curve of the artificial parameter homotopy towards one of the two more interesting stable solutions.

3.2. Alternative homotopies. Experiments with the homotopy (2) show that it converges robustly, but rather slowly. In some of our examples, more than a thousand steps (thousand evaluations of the Jacobian matrix) were needed to get to the solution. The physical interpretation provides some insight into the problem. Suppose node k has a small-signal impedance of 1 MΩ at the operating point of the circuit. The homotopy (2) implies connecting a resistor and a voltage source between this node and the ground. Before the homotopy resistor is "removed from the circuit" it should have a value at least 10 times as large as the natural impedance of the node to which it is connected. This means close to $10M\Omega$ for node k. However $\lambda/(1-\lambda)$ is equal to 10^7 only for λ *very* close to 1. We experimented briefly with a scheme

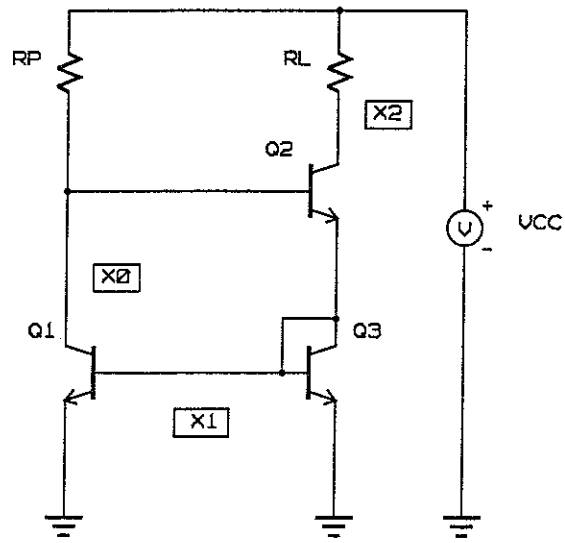

FIGURE 7. *Wilson current source.*

that attempted to scale the homotopy resistors on a per-node basis, but this became cumbersome and required *second* derivatives of device models. Instead, we propose a different approach using the general *curve tracking* option in HOMPACK. This allows a user to construct a custom homotopy. The presentation of [13] and [56] treats a homotopy of the following form:

$$\rho : \mathbf{R}^m \times \mathbf{R}^n \times [0,1) \to \mathbf{R}^n,$$

denoted $\rho(a, x, \lambda)$ where a is an m-vector, x is an n-vector, and $\lambda \in [0,1)$. The m-vector a is a random parameter. For fixed a, define

$$\rho_a(x, \lambda) = \rho(a, x, \lambda).$$

Now consider the zero set

$$\Gamma_a = \{(x, \lambda) \mid \rho_a(x, \lambda) = 0\}.$$

If certain conditions on ρ are met, then Γ_a is a union of smooth curves, one component of which connects a zero of $\rho_a(x, 0)$ with a zero of $\rho_a(x, 1)$.

In §2 we gave the homotopy first, then derived its circuit interpretation. In this section we work backwards, giving a circuit interpretation first, then deriving from it the homotopy equations. The idea is to start with all nonlinear devices removed from the circuit, then gradually bring them in. A solution trajectory is generated as the nonlinear devices sink more and more current. Figure 7 shows a Wilson current source [66].

The operating point equations for this circuit are shown below. The notation is a fragment of an executable code, and requires a bit of explanation. The transistor model `Q1` is stimulated by calling `Q1.stim` with the node voltages for the collector, base, and the emitter, respectively (note that the ground node is at 0 V by definition).

Then, a function call such as `Q1.ic()` will deliver the collector current for the given set of stimuli.

```
Q1.stim(x[0],x[1],0.0);
Q2.stim(x[2],x[0],x[1]);
Q3.stim(x[1],x[1],0.0);
F[0] = Q2.ib()+Q1.ic()+((x[0]-(VCC))/RP);
F[1] = Q3.ic()+Q3.ib()+Q2.ie()+Q1.ib();
F[2] = Q2.ic()+((x[2]-(VCC))/RL)
```

To transform these equations into a homotopy, imagine stimulating the nonlinear devices in the following fashion:

```
Q1.stim(lambda*x[0],lambda*x[1],0.0);
Q2.stim(lambda*x[2],lambda*x[0],lambda*x[1]);
Q3.stim(lambda*x[1],lambda*x[1],0.0);
```

where `lambda` $\in [0,1]$. When `lambda` $= 0$, all nonlinear devices' terminal currents are zero. Therefore, they are "removed from the circuit." This provides a starting point on a component of Γ_a, as defined above, which is tracked until $\lambda = 1$.

There is a problem with this construction for $\lambda = 0$. When $\lambda = 0$, no current flows into transistors, so they might as well be disconnected. This leaves node x_1 floating. In mathematical terms, the Jacobian matrix for the equations will be singular at $\lambda = 0$, so `HOMPACK` is not even able to start tracking the solution trajectory. We circumvented this problem by attaching extra artificial circuitry to each node. At node k, we attached a conductance of value `GLEAK` in series with a voltage source of value a_k. The voltage sources $(a_1, \ldots, a_n)$ provided the random element needed in the probability-one homotopy construction. Finally, $(1 - \lambda)$`GLEAK` approaches zero as λ approaches one. The resulting equations for the Wilson current source are:

```
double lambda_bar = 1.0 - lambda;
Q1.stim(lambda*x[0],lambda*x[1],0.0);
Q2.stim(lambda*x[2],lambda*x[0],lambda*x[1]);
Q3.stim(x[1],x[1],0.0);
rho[0] = lambda_bar*GLEAK*(x[0]-a[0])+Q2.ib()+Q1.ic()+((x[0]-VCC)/RP);
rho[1] = lambda_bar*GLEAK*(x[1]-a[1])+Q3.ic()+Q3.ib()+Q2.ie()+Q1.ib();
rho[2] = lambda_bar*GLEAK*(x[2]-a[2])+Q2.ic()+((x[2]-(VCC))/RL)
```

These equations define a homotopy $\rho(a, x, \lambda)$. Several stipulations are placed on ρ in [56] so that `HOMPACK` will be able to track the solution trajectory. We address each of these stipulations separately:

- ρ is C^2: As in homotopy (2), this depends entirely on the device models. We assume that their characteristics are sufficiently smooth.
- The Jacobian matrix $D\rho(a, x, \lambda)$ has rank n on the set

$$\rho^{-1}(0) = \{(a, x, \lambda) \mid a \in \mathbf{R}^n, 0 \leq \lambda < 1, \mathbf{x} \in \mathbf{R}^n, \rho(a, x, \lambda) = 0\}.$$

This property is assured by the terms `GLEAK*(x[k]-a[k])`. The Jacobian matrix is an $n \times (2n + 1)$ matrix. It can be written as the concatenation of three submatrices:

$$[\partial\rho/\partial a \quad \partial\rho/\partial x \quad \partial\rho/\partial\lambda].$$

The first $n \times n$ submatrix is a diagonal matrix with $-(1-\lambda)$GLEAK in each diagonal position. For $\lambda < 1$, this matrix has rank n.

- For fixed $a \in \mathbf{R}^n$, $\rho_a(x, \lambda) = \rho(a, x, \lambda)$ has a unique solution x_0 at $\lambda = 0$. When $\lambda = 0$, the equations for the Wilson current source describe a circuit consisting of resistors and voltage sources only. Setting all the currents through nonlinear devices to zero and rearranging yields the following equations for node voltages at $\lambda = 0$:

```
x[0] = (GLEAK*a[0]+VCC/RP)/(GLEAK+1.0/RP);
x[1] = a[1];
x[2] = (GLEAK*a[2]+VCC/RL)/(GLEAK+1.0/RL)
```

- $\rho_a(x, 1) = F(x)$. This holds because the "leakage" circuitry is removed and each nonlinear device is stimulated by the nominal voltage.
- The zero set Γ_a is bounded; in other words, the solution trajectory stays within some fixed distance from the origin in $\mathbf{R}^n$ for all $\lambda \in [0, 1)$. The equations represent operating point equations for a *family* of circuits, one for each value of $\lambda \in [0, 1)$. For $\lambda \in (0, 1)$ the circuit will comprise some mixture of partially stimulated nonlinear devices and the leakage circuitry from each node to ground. However, a partially stimulated nonlinear devices is still a no-gain element. This means that the entire circuit is a no-gain circuit for intermediate values of λ. Hence, the node voltages are bounded in absolute value by the sum of the absolute values of all the voltage sources in the circuit. Note that the values of the voltage sources do *not* change as λ sweeps from 0 to 1, so that a single fixed bound may be placed on the value of any node voltage in the solution trajectory.

We also make the reasonable engineering assumption that the Jacobian matrix of ρ_a has full rank at an operating point of the circuit; i.e., at a point $(x^*, 1)$ on Γ_a. This simply says that the circuit has one (or more) well defined solutions which are isolated points in $\mathbf{R}^n$.

The example of the Wilson current source indicates all the essential features of a homotopy called the *variable stimulus* homotopy. A nodal equation is written for each node that is not connected directly to a voltage source. Also, for each such node, a series combination of a conductance and a voltage source is connected to the ground. Let the voltage source have fixed value a[k] for the k-th node, and let the conductance have the value $(1 - \lambda)$GLEAK, where GLEAK is a fixed parameter. Then, for each nonlinear device, we constructed a variable stimulus model with an additional parameter $\lambda \in [0, 1]$. Each terminal voltage is multiplied by this parameter. Clearly, when $\lambda = 1$, this circuit is equivalent to the circuit whose operating point is desired. When $\lambda = 0$, the circuit is linear, with a unique value for each node voltage. Experiments with this homotopy indicate that the solution trajectories are much smoother than for (2). Moreover, the action is spread out evenly over all values of λ, rather than concentrated near the end of the path. Therefore, HOMPACK is able to take larger steps along the path and use fewer iterations.

A variation on the homotopy theme is particularly suitable to bipolar circuits, which often present the greatest challenge to operating point algorithms. Figure 4(b) shows the conventional Ebers-Moll model for a bipolar transistor, with forward current gain α_F and reverse current gain α_R. Suppose we set the gains of each transistor to $\alpha_F = \alpha_R = 0$. Each transistor transforms into a three terminal element in which a

diode is connected between the base and the collector, and the base and the emitter. This observation suggests a homotopy in which the current gain of each transistor is set to zero at $\lambda = 0$, then gradually increased towards the appropriate value for each transistor. "Floating" nodes present no problem, as with the variable stimulus homotopy, however, we still include the "leakage" circuitry to provide the random element needed to avoid bifurcations. We call this homotopy the *variable gain* homotopy.

In summary, the variable gain homotopy for bipolar circuits is a two stage procedure. Set the forward and reverse current gains of each transistor to zero. Attach a series combination of a conductance and a voltage source from each node to ground. Pick a random value for each of these voltage sources. The only nonlinear components in the resulting circuit are diodes. This circuit has a unique operating point. For phase 1, use the variable stimulus homotopy to find the operating point of this circuit. Call this operating point x^{**}. For phase 2, define the homotopy $\rho_a(x, \lambda)$ to represent the circuit with all transistor current gains multiplied by λ and all leakage conductances multiplied by $(1 - \lambda)$. The point $(x^{**}, 0)$ is clearly on a component of the zero set of the homotopy for phase 2. Now track this component as the gains of each transistor change from zero to the appropriate final value. Simultaneously let the leakage conductance become zero. The endpoint of the second phase is a point $(x^*, 1)$, such that x^* is an operating point.

As with the variable stimulus homotopy, we must address five criteria required by the probability-one theory:

- ρ is C^2. as in the previous cases, this depends entirely on the device models.
- The Jacobian matrix $D\rho(a, x, \lambda)$ has rank n along the zero curve of ρ. As in the variable stimulus homotopy, the leakage circuitry assures that the Jacobian matrix has rank n. During the second phase, in which the gain elements are brought in, the leakage conductances are allowed to go to zero, but still remain nonzero for $\lambda < 1$. Again, $D\rho$ contains a submatrix of rank n.
- For fixed $a \in \mathbf{R}^n$, $\rho_a(x, \lambda) = \rho(a, x, \lambda)$ has a unique solution x_0 at $\lambda = 0$. The starting point for the second phase is the solution x^{**} to the diode-only circuit obtained at the end of the first phase. Is this solution unique? Duffin [19] proved that a circuit consisting of voltage sources, resistors, and diodes has a unique operating point.
- $\rho_a(x, 1) = F(x)$. This is clear from the form of the equations, because the "leakage" circuitry is removed and each transistor gain is at its appropriate final value.
- The zero set of ρ_a is bounded. The theory presented in [66] shows that a bipolar transistor remains no-gain as long as the absolute value of current gains remain less than or equal to 1. This means that intermediate circuits for $\lambda < 1$ are no-gain, hence all node voltages are limited to a fixed value set by the independent sources in the circuit.

Experimental results with the variable gain homotopy are presented in the last section. For the case of bipolar circuits, a hybrid approach provides a fast solution method. Our experiments with the variable gain homotopy indicate that most of the work is spent in phase 1—that is, in finding the solution to the diode-only circuit. Duffin [19] proved that a circuit consisting of diodes as the only nonlinear components has a unique solution. (We assume the diode model includes the reverse breakdown. All practical diodes display such behavior.) Duffin's result suggests that norm-reducing

variations of Newton's method ("damped" Newton), such as proposed by Bank et al. [5], will converge robustly for such circuits. The hybrid technique, then, is to use the damped Newton code to find the operating point of the circuit with all the current gains set to zero, then employ homotopy to track the solution as the gains are restored to their desired full values. This indeed works quite well, and is two to three times faster than using homotopy alone. Performance statistics are presented in the last section.

4. Steady-state computation in the time domain. Time-domain simulations were described briefly in the introduction. A system of first order nonlinear differential equations are formulated for a circuit which contains capacitors and inductors, then standard numerical methods are employed to integrate the equations from the initial state computed using a DC operating point algorithm.

For an important class of circuits, the solution to the system of differential equations approaches a periodic steady-state asymptotically over time as initial transients die out. Unfortunately, the amount of integration steps needed to get to the steady-state can be prohibitively large. Various techniques, that result in savings in computer time and an improvement in the accuracy of the solution, have been proposed [4], [33], [58], [59], [60], [61] to calculate the steady-state response directly. One such approach is to replace the nonlinear differential equations with nonlinear difference equations, employing a numerical approximation for the derivatives [33]. Each solution waveform, assumed to be periodic, is represented as a vector of sampled values on a fixed partition of time points over one period. Thus, if there are n equations in the system of nonlinear differential equations, and m samples per period, the discretization process results in nm equations in nm unknowns. The resulting system can be large, but is very sparse.

Getting a solution to this system of nonlinear algebraic equations presents the same difficulties as finding DC operating points of a circuit. Can the artificial parameter homotopy machinery that we have developed for the operating point problem be applied to the systems of equations which arise from the steady-state problem? In this section, we answer this question affirmatively. The key idea is to prove the inner product condition for the equations that result from discretizing the differential equations.

Consider the simple one-transistor amplifier circuit of Figure 5. If the time constant established by `C1` is large compared to the period of the stimulus, finding the time-domain response of this circuit by treating it as an initial value problem is expensive. Suppose, instead, we treat this as a two-point boundary value problem. The following system of nonlinear differential equations describes the time-domain behavior of the circuit. The unknowns are periodic functions of time, e.g., $x_C(t)$ is the waveform of the collector voltage of `Q1`. The notation $i_C(x_C, x_B, x_E)$ denotes the instantaneous current flowing into the collector of `Q1`, given instantaneous voltages (x_C, x_B, x_E) of the collector, base, and emitter respectively.

$$
\begin{aligned}
(x_B - \mathtt{VCC})/\mathtt{RB1} + x_B/\mathtt{RB2} + i_B(x_C, x_B, x_E) + \mathtt{C1}\frac{d}{dt}(x_B - \cos(\omega t)) &= 0, \\
x_E/\mathtt{RE} + \mathtt{CE}\frac{d}{dt}x_E + i_E(x_C, x_B, x_E) &= 0, \\
(x_C - \mathtt{VCC})/\mathtt{RC} + i_C(x_C, x_B, x_E) &= 0.
\end{aligned}
$$

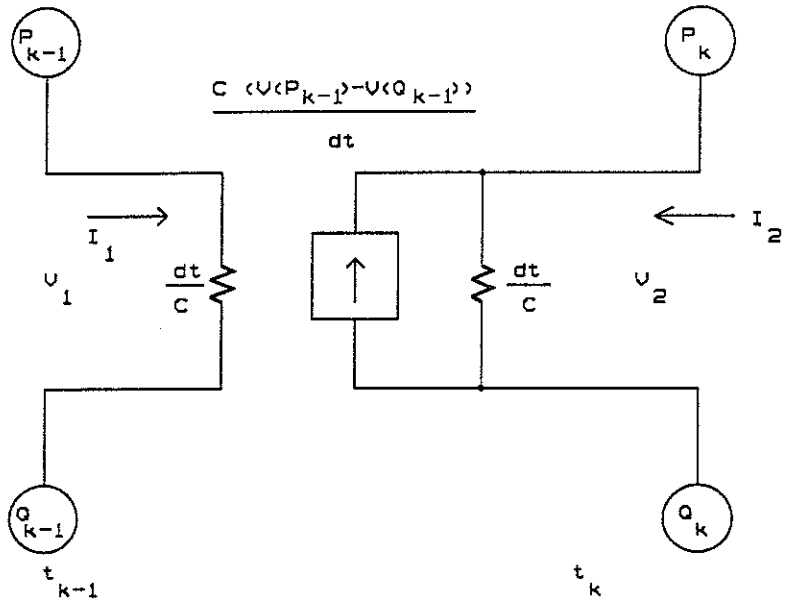

FIGURE 8. *Coupled circuits.*

The following additional conditions enforce periodicity, where T is the (known) period of the stimulus:

$$x_C(0) = x_C(T),$$
$$x_B(0) = x_B(T),$$
$$x_E(0) = x_E(T).$$

Given some convenient number of sample points, say m, the above system can be discretized on $[0,T)$ using the mesh points $0 = t_0 < t_1 < t_2 < \cdots < t_{m-1} < t_m = T$. The derivative operator dx/dt is replaced by a forward difference approximation $(x_{k+1} - x_k)/(t_{k+1} - t_k)$, where the subscripts are taken modulo m, and $x_k \approx x(t_k)$.

The result is a system of $3m$ equations in $3m$ unknowns. The equations are still nonlinear because of terms such as $i_E(x_C(t_k), x_B(t_k), x_E(t_k))$. We argue that this system of nonlinear algebraic equations are simply the *DC operating point* equations for a passive circuit. Therefore, all the global convergence arguments we have developed earlier apply. The original circuit can be copied m times, and the copies labeled as t_0, t_1, etc. Consider a capacitor between nodes P and Q in the original circuit. This capacitor can be replaced by a resistor and a voltage-controlled current source in the t_{k-1} and t_k copies as shown in Figure 8.

In the original circuit, the nodal equation for node P is

$$A + \mathrm{C}d(v_P(t) - v_Q(t))/dt,$$

to account for the current flowing into the capacitor. The term A depends on other connections to node P. Writing dt as an abbreviation for $t_k - t_{k-1}$, the nodal equation for node P in the t_k circuit is

$$A_k + \frac{\mathrm{C}}{dt}(v_P(t_k) - v_Q(t_k)) - \frac{\mathrm{C}}{dt}(v_P(t_{k-1}) - v_Q(t_{k-1})),$$

where the voltage-controlled current source introduces coupling from the previous time point t_{k-1}. This equation is the discrete approximation to the differential equation given above. The equation for node Q is similar with a sign change for the derivative term. Finally, there is a connection from copy t_0 to copy t_{n-1} to enforce periodicity.

The "unrolled" circuit of Figure 8 is a nonlinear resistive circuit, but does it satisfy the inner product condition of Theorem 1 on some r-ball? A voltage-controlled current source is a nonpassive element, therefore, we have to prove that the passivity condition is satisfied.

The circuitry in the center of Figure 8 may be treated as a component with four terminals. In circuit terminology, it is a *linear two-port.* We argue that it is a *passive* linear two-port. This implies that the entire circuit is passive, since the other components are resistors, diodes, and transistors. Let a current I_1 flow in and out of the terminals on the left side of the component, and let there be a voltage drop of V_1 across these two terminals. Define I_2 and V_2 similarly for the right-hand side. The total power dissipated by the component is $I_1V_1 + I_2V_2$. We show that this power is always nonnegative. Using Ohm's law, and the definition of the voltage-controlled current source, we may write

$$I_1V_1 = \frac{\mathtt{C}}{dt}V_1^2,$$
$$I_2V_2 = \frac{\mathtt{C}}{dt}V_2^2 - \frac{\mathtt{C}}{dt}V_1V_2,$$

which yields

$$\begin{aligned} I_1V_1 + I_2V_2 &= \frac{\mathtt{C}}{dt}V_1^2 + \frac{\mathtt{C}}{dt}V_2^2 - \frac{\mathtt{C}}{dt}V_1V_2 \\ &= \frac{\mathtt{C}}{2dt}(V_1^2 + V_2^2) + \frac{\mathtt{C}}{2dt}(V_1 - V_2)^2. \end{aligned}$$

The last quantity is clearly nonnegative for all v_1 and v_2. Thus, the discretization of the original system of differential equations produces a system of nonlinear algebraic equations that satisfies the inner product condition of Theorem 1.

5. Examples and practical results. In this section we give some practical results on some small, but difficult circuits. All of the examples are bipolar circuits. We used the Ebers-Moll model, without modeling the reverse breakdown. Our model should be close to the simple model used in `SPICE 2G6` circuit simulator [2].

5.1. Example circuits. The first circuit in our benchmark suite is a cascade of three Schmitt Trigger circuits [28]. This circuit is not particularly useful, but is a tough challenge for operating point algorithms. The output voltages of a Schmitt Trigger will switch abruptly between two extremes for a small excursion of the input voltage, called the "trigger". The two complementary outputs of the center circuit are fed through buffering resistors to the trigger inputs of copies of the same circuit, thus the number of switching possibilities multiply. If `Vx` is set below the lower trigger point, then one output of the middle circuit goes low to about 0.9 V and the complementary output goes high to about 12 V. The voltage on the low output of the center circuit is below the lower trip point of the trigger to which it is connected, and the voltage

on the high output of the center circuit is above the upper trip point of the trigger to which it is connected. Thus, the circuit has a unique operating point. However, for a supply voltage below 12 V, the circuit may still have multiple solutions.

Newton's method, as implemented in a commercial circuit simulator, is unable to get an operating point for this circuit. Moreover, continuation in the supply voltage is confused by the multiple solutions at intermediate values of the supply. Homotopy methods computed an operating point for this circuit accurate to approximately 10^{-14} A at each node.

An important class of practical circuits which also exhibit multiple operating points are bandgap voltage references (see, for example, [8]). Our second circuit is a bipolar implementation of such a reference. The convergence of a proprietary simulator depends on the initial voltage for the output node of this circuit. For certain settings, the simulator will converge to one of two operating points, at which the output is about 1.23 V (the desired value) or about 14 V. For other initial settings, the simulator does not converge. Homotopy techniques applied to this example, and starting from a variety of widely spaced starting points, exhibited robust convergence. Of the three DC solutions for this circuit, two are stable and one is unstable. In other words, if the actual circuit is placed into the unstable state, it will immediately move to one of the two stable states. Thus, the two stable solutions are of most interest to a circuit designer. In our experiments the homotopy method converged to one of the two stable solutions for any choice of the random vector. This is in contrast to Newton's method, which sometimes converges to the unstable solution.

Our third circuit is the input stage of the famous 741 operational amplifier[24] shown in Figure 9. The operation of the circuit is sensitive to the Early voltage parameter `Va` for transistors `Q5` and `Q6`. The transistor model used in our experiments does not model the Early effect, however we can mimic the effect of a large Early voltage on these two transistors by connecting large resistors in parallel between the collector and the emitter. With `RVA1=RVA2=1e12` the circuit has a very large DC gain. One "figure of merit" for a numerical implementation of an operating point algorithm is to see how large a value can be used for these resistors while still analyzing the operation of the circuit correctly.

As the input terminals are slightly unbalanced (`VPOS` $\neq$ `VNEG`), the output voltage switches abruptly from approximately 0 V to negative 12 V. In the middle of this switching region, the circuit operates as a linear amplifier with very high DC gain. The DC gain in the linear region can be estimated by forming a divided difference of two operating points in this region. Our simulation gave an estimate of $5.711 \cdot 10^9$ for the gain, compared to a hand-calculated value of $5.713 \cdot 10^9$ using a linearized model of the transistors. The same perturbation analysis using a commercial simulator produced an estimate of $4.950 \cdot 10^8$—off by a factor of 10. The commercial simulator attaches artificial conductances from each node to ground as a convergence aid; the default value of these conductances is set "large enough" so that they should not disturb the operation of the circuit. However, the gain of this circuit is so large that the presence of these artificial conductances is significant.

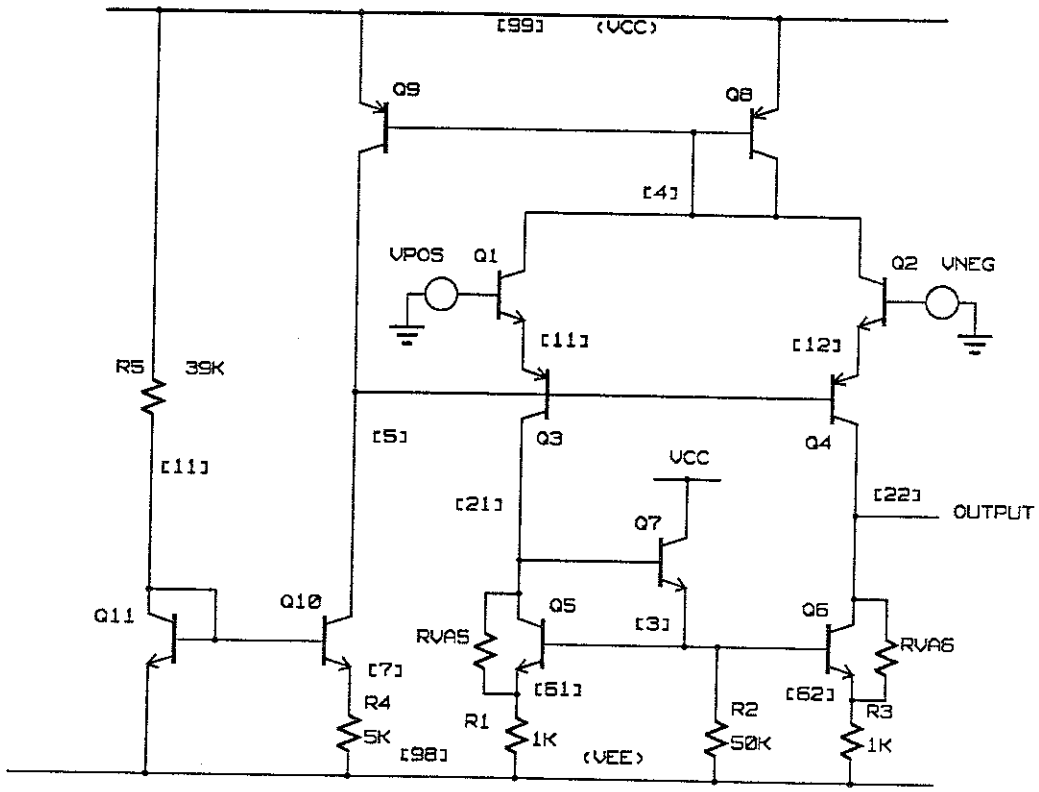

FIGURE 9. *Input stage of 741 op amp.*

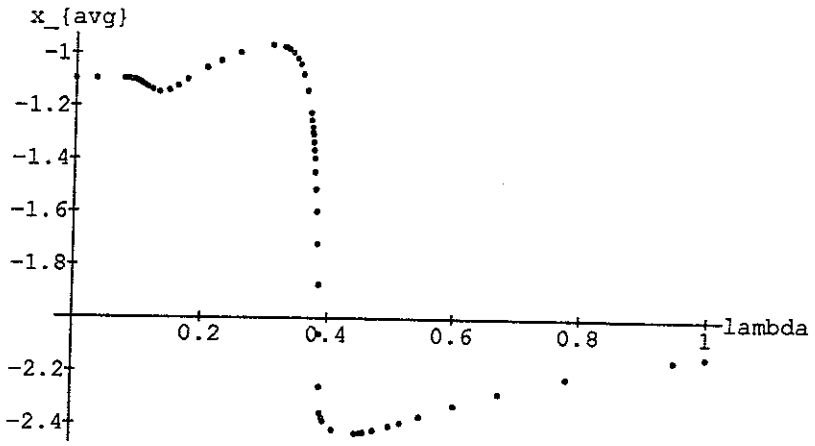

FIGURE 10. *Convergence trace.*

Figure 10 shows the HOMPACK *convergence trace* for this circuit. The computed trajectory is a path in 10-dimensional space. This figure plots the the average of these ten paths against λ:

$$x_{\text{AVG}}(\lambda) = \frac{1}{10}\sum_{k=1}^{10} x_k.$$

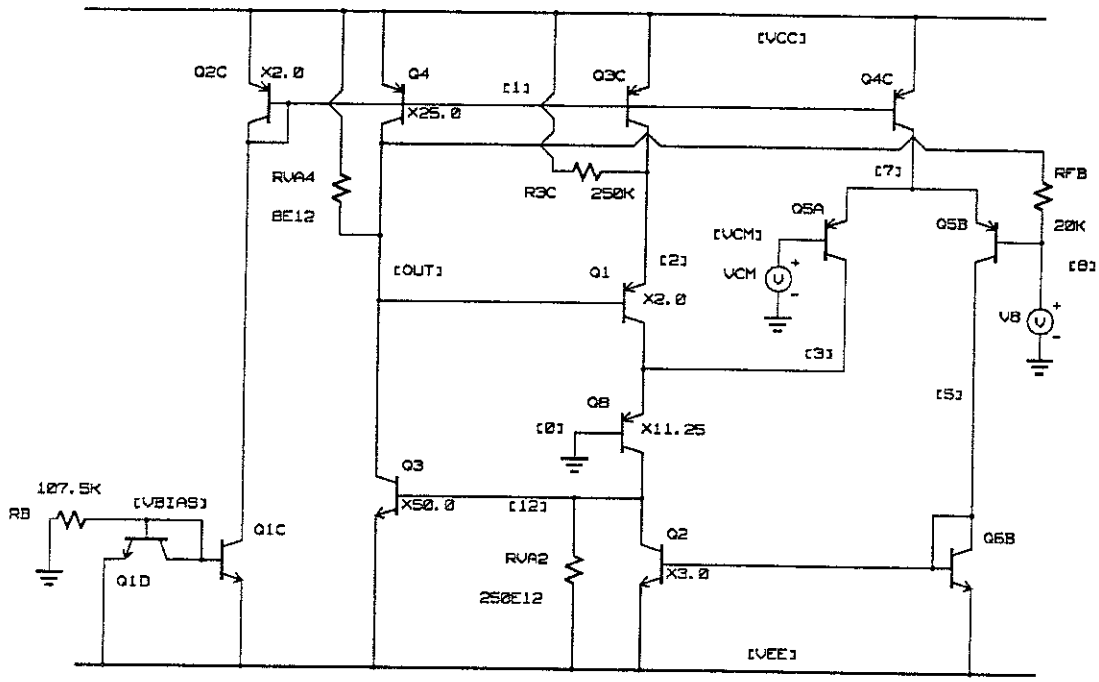

FIGURE 11. *Difficult common mode bias circuit.*

This trace can be displayed as the algorithm is working towards the solution, and can provide useful visual feedback to the designer.

Figure 11 shows a particularly difficult circuit. This is a feedback circuit used in an operational amplifier [6] with a very good common mode rejection ratio. The independent source V8 is inserted to exercise the feedback loop. For values of V8 in a small hysteresis range, the circuit has three operating points (one is unstable). A homotopy method allowed us to robustly determine the two desired (i.e., stable) solutions in the hysteresis region. In practice, this circuit behaves well, but two commercial circuit simulators failed to analyze the DC behavior of this circuit correctly.

Figure 12 is of particular interest because our techniques helped improve the design of the circuit. This circuit is another voltage reference, similar to circuit two. The operation of this circuit is described in [7]. If R5 and R6 are given slightly different values, the performance of the circuit will improve, but the possibility of multiple DC solutions arises. This is undesirable in practice, because the circuit will only function as required at one of these DC solutions. Diode-connected transistor Q10 is included as a so-called "start-up" device to force the circuit to have only the desired DC solution. Our methods were able to identify *two* stable DC solutions, even with the start-up device, when the values of R5 and R6 differed by about five percent. This information enabled the designer to estimate the manufacturing tolerances necessary for two resistors in order to ensure that the circuit would behave as anticipated.

5.2. Performance data and comparisons. Convergence and timing data were generated for the following circuits from our benchmark suite:

Cascade	Schmitt Trigger cascade;
DcNine	circuit with nine distinct solutions from [52];
Brokaw	Brokaw voltage reference circuit;

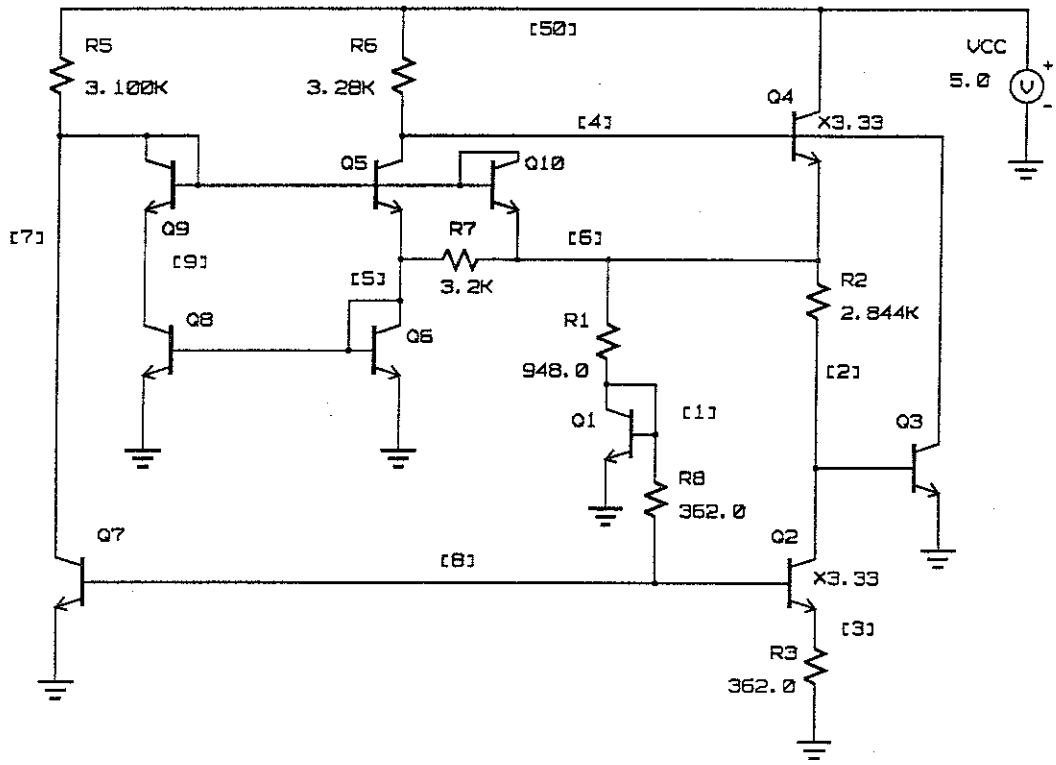

FIGURE 12. *Hybrid voltage reference.*

Hybrid	hybrid voltage reference of Figure 12;
CmMode(1)	common mode circuit of Figure 11 at edge of hysteresis region;
CmMode(2)	common mode circuit of Figure 11 in hysteresis region.

Each circuit was analyzed fifty times using values of the a parameter vector uniformly distributed between the most negative and most positive supply voltages in each particular circuit. Numerical parameters were set so that at $\lambda = 0$, the k-th node was forced to a value of a_k. Thus, the circuit was exercised over a large space of starting points. Table 1 shows convergence statistics for the above examples, using the routine `FIXPNS` from `HOMPACK` with a tracking tolerance of $1.0 \cdot 10^{-7}$ [56]. The minimum, average and maximum number of Jacobian matrix evaluations is reported for each circuit over the fifty trials. Convergence to a valid solution was obtained for every circuit from every starting point. For those circuits with multiple operating points, the homotopy method always converged to one of the two stable solutions.

The above results support the theoretical claims of global convergence. In practice, it is possible to set numerical parameters a bit differently so that convergence is achieved more quickly (in case of failure, the circuit is reanalyzed with more stringent parameter settings). Table 2 shows one sample run for each circuit with parameter settings which seem adequate for general use. Timing results were obtained on a SUN 4 workstation running Berkeley Unix.

Table 3 shows convergence statistics for the variable gain homotopy of §3.2. The data are presented in the form "phase 1 + phase 2." In phase 1, the operating point of the diode-only circuit is calculated using a damped Newton code. In phase 2, the

TABLE 1
Performance of variable stimulus homotopy.

Variable stimulus homotopy using FIXPNS.			
circuit	number of iterations		
	min	avg	max
Cascade	351	621	1299
DcNine	163	290	463
Brokaw	299	355	406
Hybrid	346	435	604
CmMode(1)	310	494	787
CmMode(2)	254	341	451

TABLE 2
Performance with normal parameter settings.

Variable stimulus homotopy using FIXPNS.		
circuit	number of iterations	time (sec)
Cascade	496	31.70
DcNine	127	7.60
Brokaw	193	8.70
Hybrid	184	7.25
CmMode(1)	277	11.80
CmMode(2)	195	7.75

TABLE 3
Performance of variable gain homotopy.

Variable gain homotopy.	
circuit	number of iterations (Newton + homotopy)
Cascade	12 + 184
DcNine	9 + 23
Brokaw	16 + 27
Hybrid	23 + 16
CmMode(1)	16 + 46
CmMode(2)	18 + 24

current gains of the transistor models are swept from 0 to their final values. It is interesting that more work is spent in phase 1 than in phase 2.

Except for the Schmitt Trigger cascade, these iteration counts are within a factor of three of the number of iterations for a damped Newton code alone. Yet the damped Newton method does not always converge, or may converge to a zero of the equations which is electronically unstable. Thus, at least in the case of bipolar transistors, we can enjoy the robust convergence of the homotopy method with quite reasonable computing cost.

5.3. Example of a steady-state computation. Consider a system of linear first-order ODEs driven by a sinusoidal forcing function. Theory shows that the solution to such a system must be sinusoidal with the same period as the driving function.

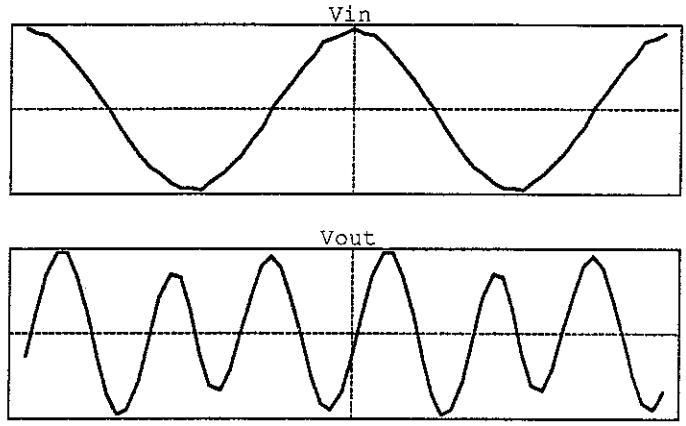

FIGURE 13. *Input and output for frequency tripler circuit.*

However, for nonlinear ODEs, the situation is much more interesting. Among other possibilities, the solution to the equations may be periodic with the frequency equal to a harmonic of the driving frequency. This effect is used in electronic circuits to generate integer multiples of a reference frequency. Figure 13 shows the input and output from such a frequency multiplier circuit [17] driven by a sinusoidal input.

We applied the discretization technique of §4 with 32 sample points per period to produce a system of algebraic equations that describe the steady-state solution of this circuit. The input and output waveforms are shown annotating the figure. The collector voltage is indeed periodic, with the period equal to one-third of the input period.

5.4. Implementation of a test platform. HOMPACK is a general curve-tracking package which has no specific knowledge of electronic circuit equations. For our numerical experiments with circuit equations we wrote a driver in the C++ language [50]. The *class mechanism* and *operator overloading* facility of C++ allows us to formulate equations in familiar notation. These expressions do not evaluate to numbers, rather each expression generates a tree data structure in memory. The leaf vertices of this tree are constants or variables introduced by the user, such as unknown node voltages. The homotopy parameter λ is a special leaf vertex. Internal vertices are labeled with arithmetic operations to be applied to the subtrees of a vertex, or labeled with the address of a subroutine which computes an arbitrary function, using the values of subtrees as arguments to the function. This arrangement allows us to form the Jacobian matrix of the homotopy map using *automatic differentiation* [25]. This is *not* a difference approximation to the derivative, nor is it symbolic differentiation such as would be computed by a symbolic manipulation program, such as MACSYMA. Instead, the chain rule is applied systematically throughout each tree to produce a numerical value for partial derivatives at the same time a numerical value is being computed for the root of each tree.

Here are the equations for the one-transistor bias circuit of Figure 3, using the variable stimulus homotopy of §3.2. This is the complete input required of the user; computation of the Jacobian matrix is automatic.

```
!lambda*(xc-ac) + q1.ic() + (xc-VCC)/RC == 0;
!lambda*(xb-ab) + q1.ib() + xb/RB2 + (xb-VCC)/RB1 == 0;
!lambda*(xe-ae) + q1.ie() + xe/RE == 0;
```

The operator "!" is defined specially for the homotopy parameter (a derived class) so that `!lambda` means `(1.0-lambda)`. The function `q1` computes the collector current for an npn transistor, given voltages on the collector, base, and emitter.

Formulating the equations in this manner let us experiment quickly with a variety of different homotopies, without the tedious and error-prone hand computation of expressions for derivatives. Some simple timing studies have shown that for each Jacobian matrix evaluated at a point of the zero curve, considerably more time is spent in HOMPACK performing linear algebra computations on the matrix than is spent in our driver constructing the derivative. Therefore, the automatic computation of derivatives is not a bottleneck.

6. Related work. In addition to the references cited in the introduction, we would like to mention some other work related to the material presented in this paper.

Yamamura et al., [68], [69], [70] have demonstrated the application of homotopy methods for finding the solutions of difficult systems of circuit equations. Their implementation concentrates on *simplicial* methods which are rather different than the technique used in HOMPACK. In particular, [70] reports impressive timing results. It is difficult, however, to make a direct comparison with our benchmark timings, because their implementation assumes that the equations are in the form of a "separable" homotopy [21]. Our equation formulation does not have such an assumption.

In [51], we prove that the inner product condition holds in case of nodal equations with grounded voltage sources. Vandenberghe et al. [53], [54] presented a similar result for a more general class of equations. Their implementation results are also based on simplicial techniques. Therefore, direct timing comparisons are difficult.

Ushida and Chua [52] discuss an algorithm along the lines of HOMPACK that was developed specifically to find the DC operating points of difficult non-linear electronic circuits. They use a homotopy similar to (2), but do not include the random element. For a certain restricted class of circuits, they prove that their method is able to find *all* the DC operating points.

7. Summary. We have demonstrated that the "coercivity conditions" required for global convergence arguments of homotopy methods are quite natural for the equations that arise in circuit simulation. Proofs are obtained by reference to powerful theorems from circuit theory. Probability one methods circumvent the numerical difficulties associated with more conventional continuation methods. In practical experiments, the use of homotopy methods has allowed us to analyze difficult circuits that can not be solved by the methods available in commercial simulation programs, and to analyze multiple solutions when they occur. The performance of our homotopies, using the numerical methods provided by HOMPACK, are fast enough for practical applications.

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REFERENCES

[1] P. Antognetti, D. O. Pederson, and H. De Man, *Computer Design Aids for VLSI Circuits*, Martinus Nijhoff, Boston, MA, 1986, pp. 69–73.

[2] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE*, McGraw-Hill, New York, 1988, pp. 13–22, 40–55.

[3] ———, *Semiconductor Device Modeling with SPICE*, McGraw-Hill, New York, 1988, pp. 13–22, 40–55.

[4] T. J. Aprille and T. N. Trick, *Steady-state analysis of nonlinear circuits with periodic inputs*, Proc. IEEE, 60 (1972), pp. 108–114.

[5] R. E. Bank and D. J. Rose, *Global approximate newton methods*, Numer. Math, 37 (1981), pp. 279–295.

[6] M. Banu, J. M. Khoury, and Y. Tsividis, *Fully Differential operational amplifier with accurate output balancing*, IEEE J. Solid-State Circuits, 23 (1988), pp. 1410-1414.

[7] T.C. Banwell, *An all-NPN hybrid voltage reference*, IEEE J. Solid-State Circuits, 26 (1991), to appear.

[8] A. P. Brokaw, *A simple three-terminal IC bandgap reference*, IEEE J. Solid-State Circuits, 9 (1974), pp. 388–393.

[9] L. E. J. Brouwer, *Über abbildung von mannigfältigkeiten*, Math. Ann., 71 (1912), pp. 97–115.

[10] K. S. Chao, D. K. Liu, and C. T. Pan, *A systematic search method for obtaining multiple solutions of simultaneous nonlinear equations*, IEEE Trans. Circuits Sys., 22 (1975), pp. 748–753.

[11] K. S. Chao and R. Saeks, *Continuation methods in circuit analysis*, Proc. IEEE, 65 (1977), pp. 1187–1194.

[12] P. Chauffoureaux and M. Hasler, *Monotonicity in nonlinear resistive circuits*, Proc. IEEE Int. Symp. on Circuits and Systems, New Orleans, LA, May, 1990, pp. 395–398.

[13] S. Chow, J. Mallet-Paret, J. A. Yorke, *Finding zeroes of maps: homotopy methods that are constructive with probability one*, Math. Comp., 32 (1978), pp. 887–899.

[14] L. O. Chua and A. Ushida, *A switching-parameter algorithm for finding multiple solutions of nonlinear resistive circuits*, Int. J. Circuit Theory Appl., 4 (1976), pp. 215–239.

[15] L. O. Chua and N. N. Wang, *On the application of degree theory to the analysis of resistive nonlinear networks*, Int. J. Circuit Theory Appl., 5 (1977), pp. 35–68.

[17] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*, Addison-Wesley, Reading, MA, 1978, pp. 6–8.

[18] W. M. Coughran, Jr., E. H. Grosse, and D. J. Rose, *CAzM: A circuit analyzer with macromodeling*, IEEE Trans. Elect. Dev., 30 (1983), pp. 1207–1213.

[19] R. J. Duffin, *Nonlinear networks IIa*, Bull. Amer. Math. Soc., 53 (1947), pp. 963–971.

[20] ECAP, *1620 Electronic Circuit Analysis Program[ECAP] [1620-EE-02X]*, IBM Application Program File H20-0170-1, 1965.

[21] C. B. Garcia and W. I. Zangwill, *Pathways to Solutions, Fixed Points, and Equilibria*, Prentice-Hall, Englewood Cliffs, NJ, 1981, pp. 1–23.

[22] I. Getreu, *Modeling the Bipolar Transistor*, Tektronix, Beaverton, OR, 1976, pp. 9–23.

[23] B. Gopinath and D. Mitra, *When are transistors passive?*, Bell Sys. Tech. J., 50 (1971), pp. 2835–2847.

[24] P. R. Gray and R. G. Mayer, *Analysis and Design of Analog Integrated Circuits, 2nd ed.*, John Wiley & Sons, New York, 1984, pp. 363–373.

[25] A. Griewank, *On automatic differentiation*, Mathematical Programming 88, Kluwer, Boston, 1989.

[26] M. Hasler and J. Neirynck, *Nonlinear Circuits*, Artech House, Norwood, MA, 1986.

[27] D. A. Hodges, *Special issue on computer aided circuit analysis and device modeling*, IEEE J. Solid-State Circuits, 6 (1971).

[28] P. Horowitz and W. Hill, *The Art of Electronics*, Cambridge University Press, Cambridge, MA, 1983, pp. 124–127.

[29] C. W. Ho, A. E. Ruehli, and P. A. Brennan, *The modified nodal approach to network analysis*, IEEE Trans. Circuits Sys., 22 (1975), pp. 504–509.

[31] H. B. Keller, *Numerical solution of bifurcation and nonlinear eigenvalue problems*, in *Applications of Bifurcation Theory*, P. Rabinowitz (ed.), Academic Press, 1977, pp. 359–384.

[32] S. Kesavan, *Topics in Functional Analysis and Applications*, John Wiley and Sons, New York, 1989, p. 219.

[33] K. S. Kundert, J. K. White, and A. Sangiovani-Vincentelli, *Steady-State Methods for Simulating Analog and Microwave Circuits*, Kluwer, Boston, 1990, pp. 55–60.

[34] E. Lahaye, *Une méthode de résolution d'une catégorie d'équation transcedantes*, C. R. Acad. Sci., 198 (1932), pp. 1840–1842.

[35] W. Mathis, *Issues in CAD tools for analog integrated circuits*, Int. J. Comput. Aided VLSI Design, (to appear).

[36] W. J. McCalla, *Fundamentals of Computer-Aided Circuit Simulation*, Kluwer, Boston, MA, 1988, pp. 53–85.

[37] R. C. Melville, Lj. Trajković, and S.-C. Fang, *Artificial parameter homotopy methods for the DC operating point problem*, IEEE Trans. Comput. Aided Design, (in submission).

[38] L. Miller, Private communications, 1990.

[39] L. D. Milliman, W. A. Massena, and R. H. Dickhaut, *CIRCUIT–A Digital Computer Program for Transient Analysis of Electronic Circuits–User's Guide*, Boeing Co., Harry Diamond Lab., Rep. AD-346-1, Jan., 1967.

[40] L. Nagel, *SPICE2: A computer program to simulate semiconductor circuits*, ERL Memorandum No. ERL-M520, Univ. of California, Berkeley, May, 1975.

[41] D. Nelson, Private communications, 1990.

[42] J. M. Ortega and W. C. Rheinboldt, *Iterative Solutions of Nonlinear Equations in Several Variables*, Academic Press, New York, 1969, pp. 161–165.

[43] S. L. Richter and R. A. DeCarlo, *Continuation methods: theory and applications*, IEEE Trans. Circuits Sys., CAS-30 (1983), pp. 347–352.

[44] A. E. Ruehli, *Circuit Analysis, Simulation and Design, Part 1*, North-Holland, New York, NY, 1986, pp. 207–234.

[45] F. M. Salam, L. Ni, X. Sun, and S. Guo, *Parallel processing for the steady state solutions of large-scale non-linear models of power systems*, Proc. IEEE Int. Symp. on Circuits and Systems, Portland, OR, May, 1989, pp. 1851–1854.

[46] A. Sard, *The measure of the critical values of differential maps*, Bull. Amer. Math. Soc., 48 (1942), pp. 883–890.

[48] M. Spivak, *Calculus on Manifolds*, Benjamin/Cummings, Boston, MA, 1968.

[49] G. Strang, *Linear Algebar and its Applications*, Harcourt Brace Jovanovich, Orlando, FL, 1988, Appendix A.

[50] B. Stroustrup, *The C++ Programming Language*, Addison-Wesley, Reading, MA, 1986.

[51] Lj. Trajković, R. C. Melville, and S.-C. Fang, *Passivity and no-gain properties establish global convergence of a homotopy method for DC operating points*, Proc. IEEE Int. Symp. on Circuits and Systems, New Orleans, LA, May, 1990, pp. 914–917.

[52] A. Ushida and L. O. Chua, *Tracing solution curves of nonlinear equations with sharp turning points*, Int. J. Circuit Theory Appl., 12 (1984), pp. 1–21.

[53] L. VANDENBERGHE AND J. VANDEWALLE, *A globally convergent algorithm for solving a broad class of nonlinear resistive circuits*, Proc. IEEE Int. Symp. on Circuits and Systems, New Orleans, LA, May, 1990, pp. 403–406.

[54] ———, *Variable dimension algorithms for solving nonlinear resistive circuits*, Proc. Eur. Conf. on Circuit Theory and Design, Brighton, UK, Sept., 1989, pp. 385–389.

[55] A. WALLACE, *Differential Topology: First Steps*, Benjamin/Cummings, Reading, MA, 1968.

[56] L. T. WATSON, S. C. BILLUPS, AND A. P. MORGAN, *Algorithm 652: HOMPACK: A suite of codes for globally convergent homotopy algorithms*, ACM Trans. Math. Software, 13 (1987), pp. 281–310.

[57] L. T. WATSON, *Numerical linear algebra aspects of globally convergent homotopy methods*, SIAM Rev., 28 (1986), pp. 529–545.

[58] ———, *An algorithm that is globally convergent with probability one for a class of nonlinear two-point boundary value problems*, SIAM J. Numer. Anal., 16 (1979), pp. 394–401.

[59] ———, *Solving finite difference approximations to nonlinear two-point boundary value problems by a homotopy method*, SIAM J. Sci. Stat. Comput., 1 (1980), pp. 467–480.

[60] L. T. WATSON AND M. R. SCOTT, *Solving spline-collocation approximations to nonlinear two-point boundary-value problems by a homotopy method*, Appl. Math. Comput., 24 (1987), pp. 333–357.

[61] L. T. WATSON AND L. R. SCOTT, *Solving Galerkin approximations to nonlinear two-point boundary value problems with a globally convergent homotopy method*, SIAM J. Sci. Stat. Comput., 8 (1987), pp. 768–789.

[62] W. T. WEEKS, A. J. JIMINEZ, G. W. MAHONEY, D. MEHTA, H. QASSEMZADEH, AND T. R. SCOTT, *Algorithms for ASTAP-a network-analysis program*, IEEE Trans. Circuits Sys., 20 (1973), pp. 628–634.

[63] G. WETTLAUFER AND W. MATHIS, *Finding all DC-equilibrium-points of nonlinear circuits*, Proc. 32nd Midwest Symp. on Circuits and Systems, Urbana, IL, 1989, to appear.

[64] A. N. WILLSON, JR., *Nonlinear Networks: Theory and Analysis*, IEEE Press, Los Alamitos, CA, 1975.

[65] ———, *The no-gain property for networks containing three-terminal elements*, IEEE Trans. Circuits Sys., 22 (1975), pp. 678–687.

[66] G. R. WILSON, *A monolithic junction FET-npn operational amplifier*, IEEE J. Solid-State Circuits, 3 (1968), pp. 341–348.

[67] J. L. WYATT, JR., L. O. CHUA, J. W. GANNETT, I. C. GONKAR, AND D. N. GREEN, *Energy concepts in the state-space theory of nonlinear n-ports: part I—passivity*, IEEE Trans. Circuits Sys., 28 (1981), pp. 48–61.

[68] K. YAMAMURA AND K. HORIUCHI, *A globally and quadratically convergent algorithm for solving nonlinear resistive networks*, IEEE Trans. Comput. Aided Design, 9 (1990), pp. 487–499.

[69] K. YAMAMURA AND M. KIYOI, *A piecewise linear homotopy method with the use of the Newton homotopy and polyhedral subdivision*, Trans. IEICE, 73 (1990), pp. 140–148.

[70] K. YAMAMURA AND K. HORIUCHI, *Solving nonlinear resistive networks by a homotopy method using a rectangular subdivision*, Proc. IEEE Int. Symp. on Circuits and Systems, Espoo, Finland, June, 1988, pp. 1225–1228.

[71] P. YANG, *Circuit simulation and modeling*, IEEE Circuits Devices Mag., 5 (1989), pp. 48–49.

[72] ———, *Circuit simulation and modeling*, IEEE Circuits Devices Mag., 5 (1989), p. 50.

[74] C. W. YUN AND K. S. CHAO, *Simple solution curves of non-linear resistive networks*, Int. J. Circuit Theory Appl., 11 (1983), pp. 47–55.